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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,764	06/26/2003	Bong-Suck Kim	053933-5045	4495

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EXAMINER	
PHAN, THIEM D	

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,764	KIM ET AL.	
	Examiner	Art Unit	
	Tim Phan	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *11-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicants' election of Group I-A, Claims 1-10, filed on 9/12/05 is acknowledged.

The Restriction mailed on 8/12/05 has been carefully reviewed and is held to be proper. Applicants did not distinctly and specifically point out any logical error in the Restriction Requirement. Moreover, due to the lack of traversal on the merits, Applicants' election of Group I-A, claims 1-10, has been treated as an election without traverse.

Accordingly, Claims 11-17 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group, there being no allowable generic or linking claim.

The Restriction filed on 8/12/05 is hereby **made Final**.

Applicants are required to cancel these nonelected claim (11-17) or take other appropriate action.

An Office Action on the merits of Claims 1-10 now follows.

Specification

2.

- On page 1, before "BACKGROUND OF THE INVENTION", insert:

"CROSS REFERENCE TO RELATED DOCUMENT

This application claims priority to Korean Patent Application No. 2002-79216, filed on December 12, 2002.".

- The following title is suggested: "Method for Manufacturing a Built-up Printed Circuit Board with Stack Type Via-holes".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizumoto et al (US 5,956,843) hereinafter '843 in view of Asai et al (US 6,240,636) or vice versa.

As applied to claim 1, Mizumoto et al teach a method of making multilayer printed

wiring board, comprising:

- (a) forming a first via-hole (Fig. 2, 130) through a first laminated sheet (Fig. 2, 110) by etching (Col. 1, lines 50-54);
- (b) forming a first plated layer (Fig. 15, 540) on a first via-hole and on a first laminated copper sheet (Fig. 15, 520);

- (c) filling the first plated via-hole with a via-hole filling material (Fig. 17, 550);
  (d) grinding the top surface (Fig. 18, 530; col. 5, lines 48-50) of the first via-hole filled with the via-hole filling material to level the first via-hole.
- (e) forming a second plated layer (Fig. 13, 390on the first filled via-hole and the first plated layer to cover the first filled via-hole; and
- (f) disposing a second laminated sheet (Fig. 13, 320) on the second plated layer, and
- repeating the steps (a) to (e) to form a second via-hole.

Asai et al teach a method of producing vias in printed circuit board, comprising:

- (a) forming a first via-hole (Fig. 1, 5) through a laminated copper sheet or the like (Fig. 1, 1) by means of a laser drill or ablation (Fig. 1).

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the forming of a via-hole through a laminated copper sheet by laser ablation, as taught by Asai et al and not their general structure, to the method of

making multilayer printed wiring board by Mizumoto et al in order to speed up the making of a via-hole by laser drilling process.

As applied to claim 2, Asai et al teach that the laser is a CO.sub.2 laser (Fig. 1).

As applied to claim 3, Asai et al teach that the plated layers are formed by means of electroless plating or electroplating.

As applied to claim 4, Mizumoto et al teach that the via-hole filling material is filled in the via-hole by a general screen printing process with a squeegee (Fig. 17, 550; col. 5, lines 42-46).

As applied to claim 5, Mizumoto et al and Asai et al teach a method of making multilayer printed wiring board, which reads on applicants' claimed invention, except for having a portion of a poly screen corresponding to the via-hole opened so that the via-hole filling material passes through the opened portion to fill all the via-hole during the screen printing.

It is mere matter of design choice to have a portion of a poly screen corresponding to the via-hole opened so that the via-hole filling material passes through the opened portion to fill all the via-hole during the screen printing and it appears that the invention would perform well with spot-filling the via-hole since it is known in the art that only the via-hole is spot-filled by covering the outer portions of the via hole (Mizumoto et al, col. 5, lines 37-41).

As applied to claim 6, Mizumoto et al teach that the via-hole filling material is liquefied insulating resin or paste (Col. 5, lines 13-18).

As applied to claim 7, Mizumoto et al teach that the via-hole filling material is conductive or metal paste (Col. 5, line 13).

As applied to claim 8, Mizumoto et al teach that the conductive paste is copper paste (Col. 4, line 65).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizumoto et al in view of Asai et al and further view of Ogura et al (US 6,660,811).

Mizumoto et al and Asai et al teach a method of making multilayer printed wiring board, which reads on applicants' claimed invention, except for having a viscosity of the via-hole filling material no more than 100 dPa.s.

Ogura et al teach a novel epoxy resin of condensed aromatic rings used in printed wiring board with a melt viscosity of 5dPa (Col. 2, line 7) in order to have flame retardation and heat resistant characteristics.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the three teachings by applying the novel epoxy resin, as taught by Ogura et al, to the making of PCB as taught by Mizumoto et al and Asai et al in order to bring the flame retardation and heat resistant characteristics to the PCB.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizumoto et al ('843) in view of Asai et al and further view of Mizumoto et al (US 5,883,335) hereinafter '335.

The '843 and Asai et al teach a method of making multilayer printed wiring board, which reads on applicants' claimed invention, including the grinding of the top surface (The '843, fig. 18, 530; col. 5, lines 48-50) of the first via-hole filled with the via-hole filling material to level the first via-hole; except for disclosing a grinder made of ceramic buff, scotch buff, highcut buff, or belt.

The '335 teaches a process of making a printed circuit board for integrating a chip component with the through holes being filled up by screen printing and being grinded by a belt sander or buff grinding in order to smooth the surface.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the three teachings by applying the belt sander or buff grinding, as taught by the '335, to the making of PCB as taught by the '843 and Asai et al in order to smooth surface of the filled via-holes.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M - F, 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A. DEXTER TUGBANG
PRIMARY EXAMINER

Tim Phan
Examiner
Art Unit 3729

tp
October 14, 2005